CLAIMS

What is claimed is:

1. A method for generating a data clock having edge coincidence with an aggregate PN code, the method comprising the steps of:

providing an aggregate PN code generator having an epoch output;

providing a PN master clock;

providing a PN master clock divisor N_c;

driving a data clock generator with the PN master clock, and the PN master clock divisor; and

resetting the data clock generator when the aggregate PN code generator generates an epoch signal.

2. A method as in claim 1 wherein the step of providing the aggregate PN code generator having an epoch output further comprises the step of:

providing a plurality of PN subcomponent code generators, wherein each of the plurality of PN subcomponent code generators generate PN codes whose prime factors are unique from each of the other PN codes, and wherein at least two of the plurality of PN subcomponent codes have at least one common epoch point.

3. A method as in claim 2 wherein the step of providing the plurality of PN subcomponent code generators further comprises the steps of:

one of the plurality of PN subcomponent code generators generating a binary code 2^n, for n=0,1,2,3, ... k, where k is predetermined; and

another one of the plurality of PN subcomponent code generators generating a maximal length code 2^m-1, for m ≤ n.

4. A method as in claim 3 wherein the step of providing the PN master clock divisor N_c further comprises the steps of:

prime factorizing the maximal length code 2^m-1, for m ≤ n;

generating the PN master clock divisor N_c according to 2^n, or 2^n multiplied times a prime factor or prime factor multiple in accordance with the prime factorizing of the maximal length code 2^m-1.

5. A method as in claim 4 wherein the step of generating the PN master clock divisor N_c further comprises the step of generating the PN master clock divisor according to a predetermined step relationship.

6. A method as in claim 5 wherein the step of generating the PN master clock divisor N_c according to a predetermined relationship further comprises the step of generating the PN master clock divisor N_c according to a log-linear step relationship.

7. A method as in claim 2 wherein the step of providing the PN code generator further comprises the step of resetting a binary divider when the common epoch point occurs.

8. A system for generating a data clock synchronous with PN component code minor epochs, the system comprising:

a first PN code generator for generating a first PN code comprising a binary code 2^n, where n=0,1,2,3,...k, and where k is predetermined;

a second PN code generator for generating a second PN code comprising a maximal length code 2^m-1, where integer $m \leq k$ and where the maximal length code has at least one maximal length code epoch in common with at least one binary code epoch;

a data clock generator, the data clock generator comprising;

an input PN master clock port

a divisor generator for generating divisor N_c; and

a binary divider coupled to the divisor generator and the first and second PN code generators, wherein the binary divider divides a PN master clock signal received on the input PN master clock port in accordance with divisor N_c and resets with the common occurrence of the maximal length code epoch and the binary code epoch.

9. A system as in claim 8 further comprising a third PN code generator, the third PN code generator generating a third PN code having prime factors not common with either the first PN code generator or the second PN code generator.

10. A system as in claim 8 wherein the divisor generator comprises a divisor N_c look-up table.

11. A system as in claim 9 further comprising a PN code combiner.

12. A system as in claim 11 wherein the PN code combiner comprises a MAND code combiner for combining the first (X), second (Y), and third (Z_1) PN codes to produce the PN composite code p(t) according to:

$$X \oplus (Y \bullet Z_1).$$

13. A system as in claim 11 wherein the PN code combiner comprises a MAJ code combiner for combining the first (X), second (Y), and third (Z_1) PN codes to produce the PN composite code p(t) according to:

$$(X \bullet Y) \oplus (Y \bullet Z_1) \oplus (X \bullet Z_1).$$

14. An integrated circuit (IC), the IC comprising:

a first PN code generator for generating a first PN code comprising a binary code 2^n, where n=0,1,2,3,...k, and where k is predetermined;

a second PN code generator for generating a second PN code comprising a maximal length code 2^m-1, where integer $m \leq k$ and where the maximal length code has at least one maximal length code epoch in common with at least one binary code epoch;

a data clock generator, the data clock generator comprising;

an input PN master clock port

a divisor generator for generating divisor N_c; and

a binary divider coupled to the divisor generator and the first and second PN code generators, wherein the binary divider divides a PN master clock signal received on the input PN master clock port in accordance with divisor N_c and resets with the common occurrence of the maximal length code epoch and the binary code epoch.

15. An IC as in claim 14 further comprising an on-chip master PN clock.

16. An IC as in claim 14 further comprising a third PN code generator for generating a third PN code, wherein primary factors of the third PN code are not common with primary factors of the first or second PN codes.

17. An IC as in claim 14 further comprising an on-chip PN code combiner for combining PN codes generated by the PN code generators.

18. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for generating a data clock having edge coincidence with an aggregate PN code, the method comprising the steps of:

providing an aggregate PN code generator having an epoch output;

providing a PN master clock;

providing a PN master clock divisor N_c;

dividing the PN master clock by the PN master clock divisor to generate a data clock;

and resetting the data clock when the aggregate PN code generator generates an epoch signal through the epoch output.

19. A program storage device as in claim 18 wherein the program of instructions comprise at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.

20. A direct sequence spread spectrum system, the system comprising:

a transmitter, wherein the transmitter comprises:

a first PN code generator for generating a first PN code comprising a binary code 2^n, where n=0,1,2,3,…k, and where k is predetermined;

a second PN code generator for generating a second PN code comprising a maximal length code 2^m-1, where integer $m \leq k$ and where the maximal length code has at least one maximal length code epoch in common with at least one binary code epoch;

a third PN code generator for generating a third PN code, wherein primary factors of the third PN code are not common with primary factors of the first or second PN codes;

a data clock generator, the data clock generator comprising;

an input PN master clock port

a divisor generator for generating divisor N_c;

a binary divider coupled to the divisor generator and the first and second PN code generators, wherein the binary divider divides a PN master clock signal received on the input PN master clock port in accordance with divisor N_c and resets with the common occurrence of the maximal length code epoch and the binary code epoch;

a receiver, wherein the receiver comprises:

a fourth PN code generator for generating the first PN code comprising the binary code 2^n, where n=0,1,2,3,...k, and where k is predetermined;

a fifth PN code generator for generating the second PN code comprising the maximal length code 2^m-1;

a sixth PN code generator for generating the third PN code, wherein primary factors of the third code are not common with primary factors of the first or second PN codes;

a second data clock generator, the second data clock generator comprising;

a second input PN master clock port

a second divisor generator for generating the divisor N_c; and

a second binary divider coupled to the second divisor generator and the fourth and fifth PN code generators, wherein the second binary divider divides a second PN master clock signal received on the second input PN master clock port in accordance with second divisor N_c and resets with the common occurrence of the maximal length code epoch and the binary code epoch.